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AN IMPROVED FLIGHT DATA TRANSCRIBER

A.J. FARRELL

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A.J. FARRELL

SUMMARY

A unit is described which converts serial data recorded on the
MKI or MKII Aero. Division Airborne Data Acquisition Package into a
form suitable for recording on 7-track computer compatible tape. It
is an improved version of a previous unit designed to work with the
MKI Data Acquisition Package.

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16. ABSTRACT:

A unit is described which converts serial data recorded on the MKI or MKII Aero. Division Airborne Data Acquisition Package into a form suitable for recording on 7-track computer compatible tape. It is an improved version of a previous unit designed to work with the MKI Data Acquisition Package.

CONTENTS

1. INTRODUCTION

For the validation of the RAN SEAKING mathematical model, a flight package [1] was designed and constructed which recorded digital data in serial form on a two track magnetic tape recorder. To convert these data into a form suitable for computer processing, a transcription unit was built [2] which transformed the serial data into parallel form and recorded them on a computer compatible tape recorder operating in the incremental mode.

In practice, this transcription method proved to be unwieldy, time-consuming and prone to human error. The incremental recording mode was limited in speed, and each of the two serial data tracks had to be transcribed separately. In addition, the computer software to manipulate the data files was cumbersome.

This memorandum describes a new transcriber which has been designed and built to overcome these deficiencies with the added capability of being able to handle data from the existing MKI or the proposed MKII flight packages with relatively minor modification. The improved transcriber is eight times faster in operation than the old version, is less prone to human error because of the simplified controls, and the associated computer handling software is simple and more efficient.

The following sections describe the operation of the unit in outline and in detail, its construction and the operating procedure.

2. OUTLINE OF OPERATION

Data are recorded by the flight package in serial form on a NAGRA IV-SJ tape recorder in the format shown in Fig. 1. The RACAL T5000 tape transport records data in 6-bit parallel form. The transcriber, therefore, has to decode the serial data from both tracks in parallel form, rearrange the data into 6-bit bytes in a fixed order and clock the bytes onto the RACAL tape transport, with appropriate gaps, as required by the computer.

Referring to the simplified block diagram Fig. [2] , the replayed signal from the two NAGRA recorder tracks is decoded to provide a stream of 12-bit parallel words from each track, together with pulses corresponding to the inter-word and inter-frame gaps from track 2 only. An inter-word gap (IWG) indicates that the two 12-bit words from tracks 1 and 2 are available at the decoder output. In response to the IWG pulse, the input control circuit switches the byte selector to divide the two 12-bit words into four 6-bit bytes, and clock these bytes into a first-in first-out (FIFO) memory stack. When 384 bytes have been input (i.e. eight frames of input data), the input

control sends a command to the output control which then outputs all 384 bytes to the RACAL tape recorder, and follows with an inter-record gap (IRG). The figure of 384 was chosen for convenience in the data handling by the computer.

The transcription process starts and stops in response to front panel push-button controls. To check the system, synthetic data from a test generator may be used in place of the decoded data. The logic used throughout is standard transistor-transistor logic (TTL) with the exception of the FIFO memory.

The following sections describe the operation of the various sections in more detail.

3. DETAILED DESCRIPTION OF OPERATION

3.1 Decoding

The unit can be arranged to accept data in three different formats, namely, MKI binary pulse amplitude modulation (BPAM) encoded data, MKI Harvard (Bi-phase mark) encoded data and MKII Harvard encoded data. The first two are alternative encoding formats from the current flight package, and one described in detail in reference 1. The third is the proposed standard for the improved MKII flight package, and is the same as the MKI Harvard but at twice the data speed. The output from each of the different forms of decoder is the same - two 12-bit parallel words, with a simultaneous IWG pulse, and an IFG pulse at the end of each 12-word frame.

3.2 Input Control Circuit

The input control circuit, using the IWG and IFG pulses for timing, generates the byte selector address, the FIFO input clock, and the commands to start the RACAL tape recorder and to start unloading the FIFO memory.

The circuit comprises three sections, the first part being the byte selector address and FIFO input clock generator. From Figs. 3(a) and 4(a), before the arrival of an IWG pulse, the circuit is inhibited. On arrival of an IWG pulse, the counter is reset, D1 becomes low (i.e. a TTL logical '0'), $\overline{D1}$ becomes high (i.e. the invert of D1 becomes a TTL logical '1') allowing the oscillator pulses through the AND gate to the counter clock input. The count sequence until D1 goes high provides the required addresses and clocks. D1 high inhibits counting until the next IWG pulse.

The second part of the circuit inhibits the IWG pulses until the start of a frame. This is to ensure that the start of a memory block is always the start of a data frame. From Figs. 3(b) and 4(b), when the front panel 'START' button is pushed, flip-flops FF1 and FF2 are preset, and the OR gate output is high, so no IWG pulses can pass through the OR gate. On the first IFG pulse, FF1, which is connected as a latch, flips, enabling FF2. On the first IWG pulse following the first IFG pulse, FF2 flips, enabling the IWG pulse stream to pass through the OR gate.

Part 3 of the input control circuit counts the input data, and, at the appropriate time, initiates the data output sequence onto the RACAL tape recorder. Referring to Figs. 3(c) and 4(c), when the front panel 'START' button is pushed, binary counter II is reset. On the eighth IFG pulse after the release of the 'START' button, D3 goes high, starting the sequence of unloading data bytes from the FIFO memory into the RACAL recorder [see Section 3.4] D3 going low clocks FF3, so that Q3 goes high. If the six-channel quick look unit [3] is operating, this puts a 'transcription in progress' mark on the chart recorder. As Q3 goes high, Q3 goes low, and this starts the tape moving on the RACAL recorder. The binary counter II resets at the combination D3.IWG (where the dot signifies a logical AND function) shortly after D3 goes high. On reset, binary counter II restarts counting. Flip-flop FF3 is connected as a latch and does not clear until the front panel 'STOP' button is pushed. When 'STOP' is pushed, the output control circuit [Section 3.4] transmits an 'AUTO STOP' level change via an OR gate and invert to clear FF3. Q3 goes low to end the 'transcription in progress' mark on the chart record, and Q3 goes high to stop the RACAL recorder tape movement. Binary counter II continues to count, but no data will be recorded.

All three parts of this circuit are mounted on printed circuit cord 57/322.

3.3   Byte Selector

The function of this circuit is to take the two 12-bit parallel words at the output of the decoder, and arrange them into four 6-bit bytes at the input to the FIFO memory stack. From Fig. 5, as the address lines change, the output bytes change according to the table.

The byte selector is made up from three standard National Semiconductor DM74153 dual 4:1 multiplexers, and is mounted on printed circuit cord 57/321.

3.4   Output Control Circuit

The basic function of this circuit is to output the data stored in the FIFO memory onto the RACAL tape recorder. It provides the FIFO output clock, the RACAL input clock, inter-record gap (IRG) and end-of-file (EOF) commands, and the 'auto stop' control for the input control circuit. (Section 3.2). For convenience, the circuit operation is discussed in two parts.

From Figs. 6 and 7, the write start line (from the input control circuit) initially goes low, triggering monostable 1 for a 4 millisecond (ms) delay to allow the RACAL recorder to get up to speed. (952,5 mm/sec.). The trailing edge of the monostable pulse (QM1) clocks Q4 of flip-flop FF4 high, which in turn enables flip-flop FF5. The first negative clock edge from the oscillator clocks Q5 high, allowing the oscillator pulses through the NAND gate. (This sequence is to ensure full length leading clock cycles). The gated oscillator output, after inversion, becomes the RACAL data input clock (positive edges) and the FIFO data output clock (negative edges). The byte counter counts 384 output bytes and resets itself, FF4 and FF5 via a delay monostable (QM2). The trailing edge of the monostable pulse also triggers the RACAL gap pulse (see next paragraph).

Part 2 of the circuit generates the IRG and EOF pulses for the RACAL recorder and the 'auto stop' pulse for the input control circuit to stop the RACAL tape motion. From Figs. 8 and 9, before the front panel 'STOP' button is pushed, QM4 is low and the gap pulse (part 1, above) is steered to the IRG output to generate the inter-record gaps on the RACAL tape. Q6 of flip-flop FF6 is cleared to low by the 'START' button being pushed, and FF6 is inhibited from flipping by QM4 being low. When the 'STOP' button is pushed, QM4 goes high, steering the next gap pulse to the EOF output, thus generating an end-of-file on the RACAL tape. QM4 being high enables FF6, so that the trailing edge of the RACAL 'busy' signal due to the EOF generation clocks Q6 low and via the input control circuit, part 3 (Section 3.2) stops the RACAL tape motion.

The output control circuit is mounted on printed circuit board 57/323(R1).

For satisfactory operation of the RACAL recorder, it has been found necessary to include a RACAL anti-ringing circuit [Fig. 54(a) of ref. [4]] in the data input clock and IRG lines to the recorder.

3.5   FIFO Stack

The first-in first-out (FIFO) memory stack accumulates the 6-bit data bytes from the byte selector output until a complete block of 384 bytes (i.e. 8 data frames) is stored. Then the entire block is output to the RACAL tape recorder. The output clock is timed to give a data packing density on the tape of 556 bits per inch (bpi).

A data byte at the FIFO input is accepted and stored in the FIFO when a negative edge occurs in the FIFO input clock. A negative edge of the output clock clears the existing data in the FIFO output register and loads the following byte. Successive output clocks output the data bytes in the order in which they were entered. The input and output operations are completely independent of each other.

The FIFO stack contains 448 memory locations, so the 384 bytes in a block can be comfortably accommodated. The stack consists of 14 Fairchild type 3341 FIFO chips mounted on printed circuit board 57/331. The chips are interconnected in accordance with the manufacturers' recommendations.

3.6   Test Generator

The test generator provides test data, IWG and IFG signals as a convenient method of checking the unit and the RACAL recorder. The circuit is described in two parts.

In part 1 (Fig. 10) is an oscillator from which all the test signals are derived. When the front panel 'START' switch is depressed, flip-flop FF7 is cleared, and the low Q7 inhibits the oscillator output. The first negative oscillator clock edge after the release of the start switch sets Q7 high and allows the clock pulses, via the NAND gate and the inverter, to trigger monostable 5. The 30 microsecond QM5 output pulses are the test IWG pulses. The $\overline{QM5}$ output clocks a 12-bit binary counter, the output of which is the Track 1 (TR1) test data (B0 to B11). The logical compliment (invert) of the counter output is the Track 2 (TR2) test data ($\overline{B0}$ to $\overline{B11}$).

To simulate the format of the flight recorder data, it is required to insert a gap after each group of twelve IWG pulses and to generate an IFG pulse in that gap. This is achieved by part 2 of the test generator circuit (Figs. 11 and 12). The logical combination C8.D8 inhibits the test IWG pulses while $\overline{C8.D8}$ enables monostable 6. The next positive going edge of B8 generates the test IFG pulse (QM6). Parts 1 and 2 are mounted on printed circuit board 57/330.

3.7   Power Supplies

The required +5 and -12 volt supplies for the unit are drawn from two outputs of an Instrumentation Group (Aerodynamics Division) standard triple regulated power supply mounted on printed circuit board 57/162(R1), with its associated transformer mounted on the unit chassis.

4.   MECHANICAL CONSTRUCTION

The unit is mounted in a standard ELNASET card frame (482,6 mm wide X 416 mm deep X 175 mm high). It is usually bolted in a rack with the RACAL T5000 tape recorder, the six-channel Quick Look system and its associated chart recorder. The Kudelsui NAGRA IV-SJ tape recorder is usually mounted in front of the unit in a special cradle to prevent accidental tape erasure. The general layout of the unit is shown in Fig. 13.

5.   OPERATING PROCEDURE

The following is a suggested operating procedure assuming the unit is mounted, as it usually is, in the Quick Look rack. It is recommended that the six-channel Quick Look unit and chart recorder be used in conjunction with the transcription unit, as the chart record aids in the interpretation of the transcribed record.

1.   Clean NAGRA and RACAL tape recorder heads with metholated spirits.

2.   Switch on all equipment. If possible, leave the RACAL recorder on for 30 minutes to reduce possibility of vacuum column failures.

3.   Load RACAL and NAGRA recorders with tape (refer to appropriate operating manuals). NAGRA recorder MUST be in transcription cradle.

4.   Zero chart recorder pens and select desired sensitivity and chart speed (refer OFFNER Dynograph model 504A manual).

5.   Select data channels to be displayed on chart by setting select switches on six-channel quick look unit |3|.

6.   Select required section of NAGRA tape.

7.   Set RACAL recorder to 'OPERATE'.

8. Start chart recorder and set NAGRA recorder to 'REPLAY'/with loudspeaker.

9. Transcribe data as required; push 'START' button to start and 'STOP' button to stop. The transcription mark will appear on the chart recorder.

10. When NAGRA tape passage has been completed, proceed to the next section of tape, repeating steps 5 to 9 above.

11. On completion of transcription, rewind NAGRA and RACAL tape, suitably labelled, to the computer centre.

12. Switch off all equipment.

6. CONCLUSION

The unit described in this memorandum forms an essential part of the data reduction equipment for the Aerodynamics Division MKI Airborne Data Acquisition Package. The improved performance in terms of speed and ease of operation compared with the previous model transcriber is particularly marked, and no further development of this unit is anticipated at this stage.

Detailed circuits and inter-wiring diagrams for the unit are available from the author.

REFERENCES

1. 'The Aerodynamics Division Airborne Data Acquisition Package MKI', A.J. FARRELL, Aerodynamics Note 386, 1979.

2. 'A Data Transcriber for the Aerodynamics Division Flight Data Acquisition System', A.J. FARRELL and D.T. HOURIGAN, Aerodynamics Technical Memorandum 310, May 1978.

3. 'A Six-Channel Quick-Look Unit for the Aerodynamics Division MKI Airborne Data Acquisition Package', A.J. FARRELL, S.H. CREED, I.M. KERTON and P. FERRAROTTO (in draft).

4. 'T5000 Incremental Recording System Technical Handbook', RACAL-THERMIONIC LTD, HYTHE, SOUTHAMPTON, ENGLAND, 1971.
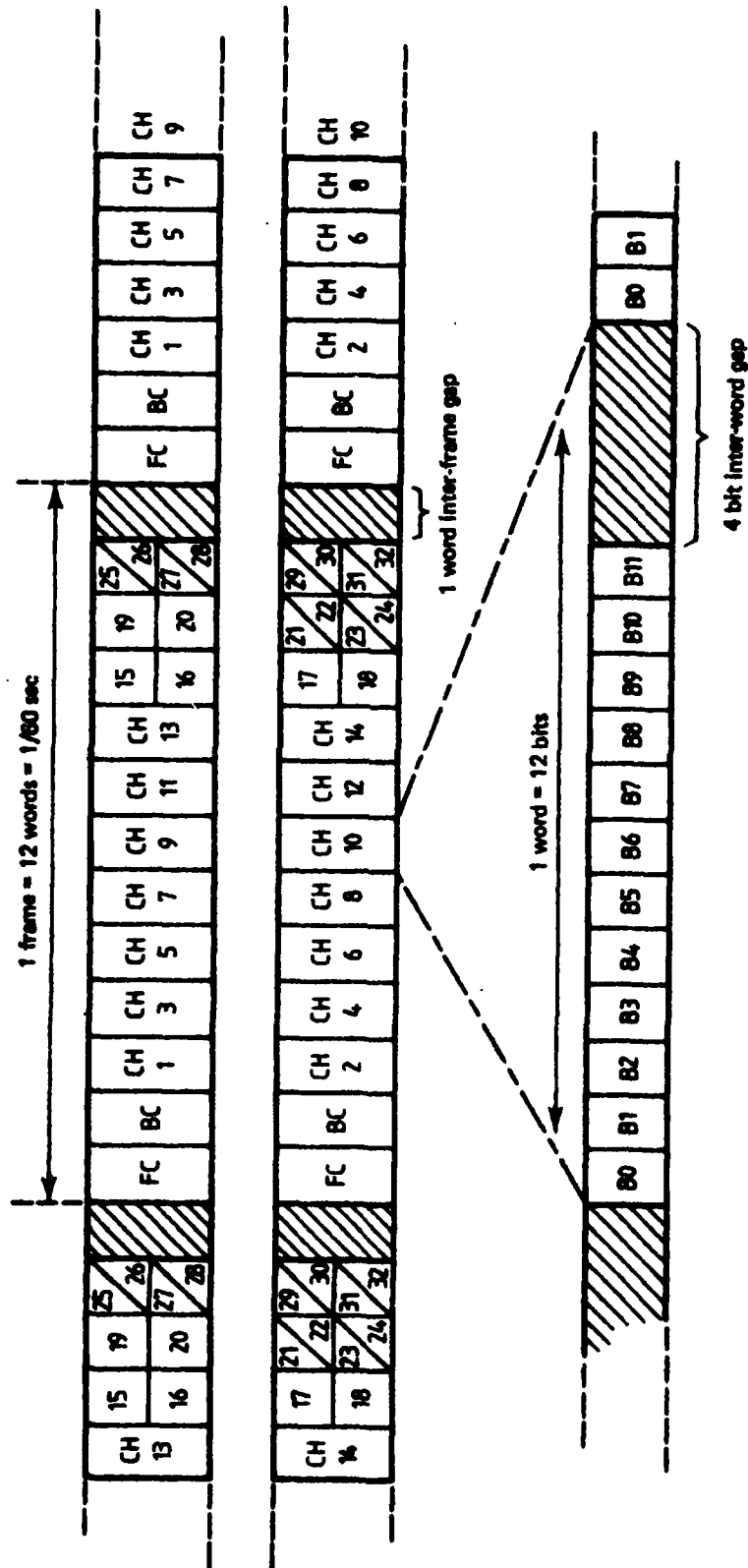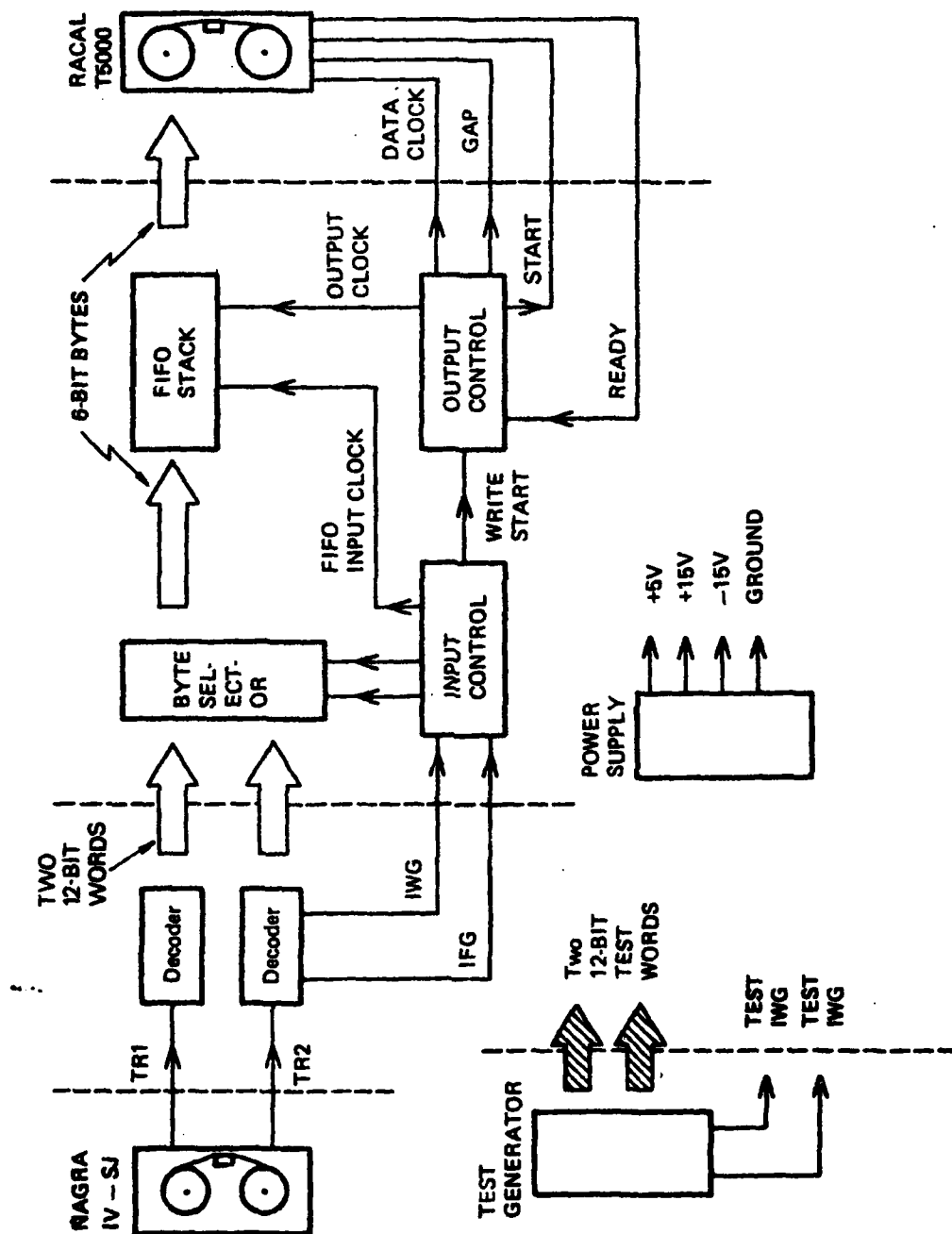
FIG. 1 RECORDING FORMAT

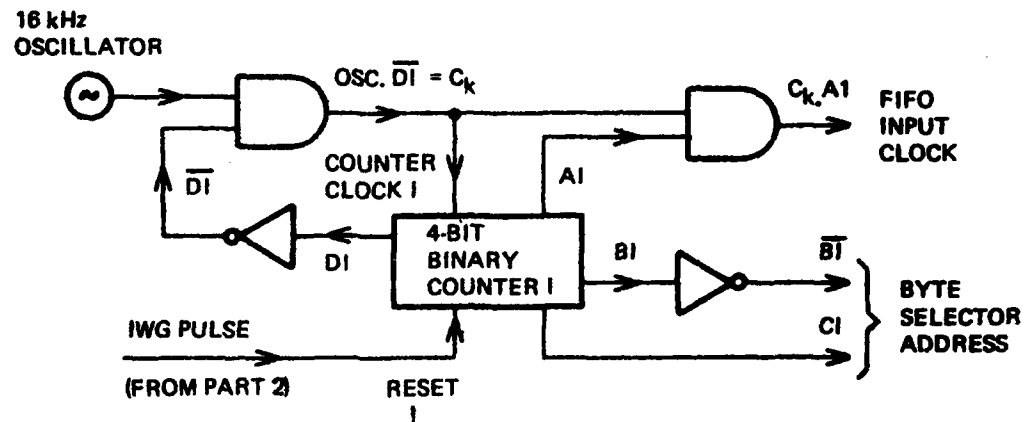FIG. 2   SIMPLIFIED BLOCK DIAGRAM
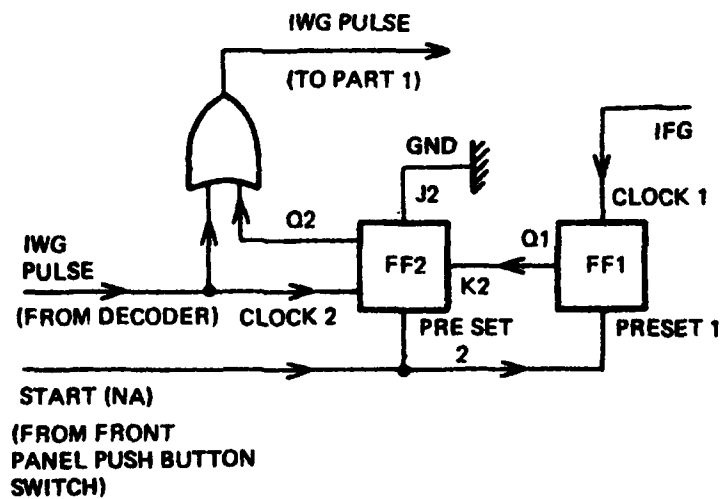
FIG. 3(a) INPUT CONTROL CIRCUIT — PART I

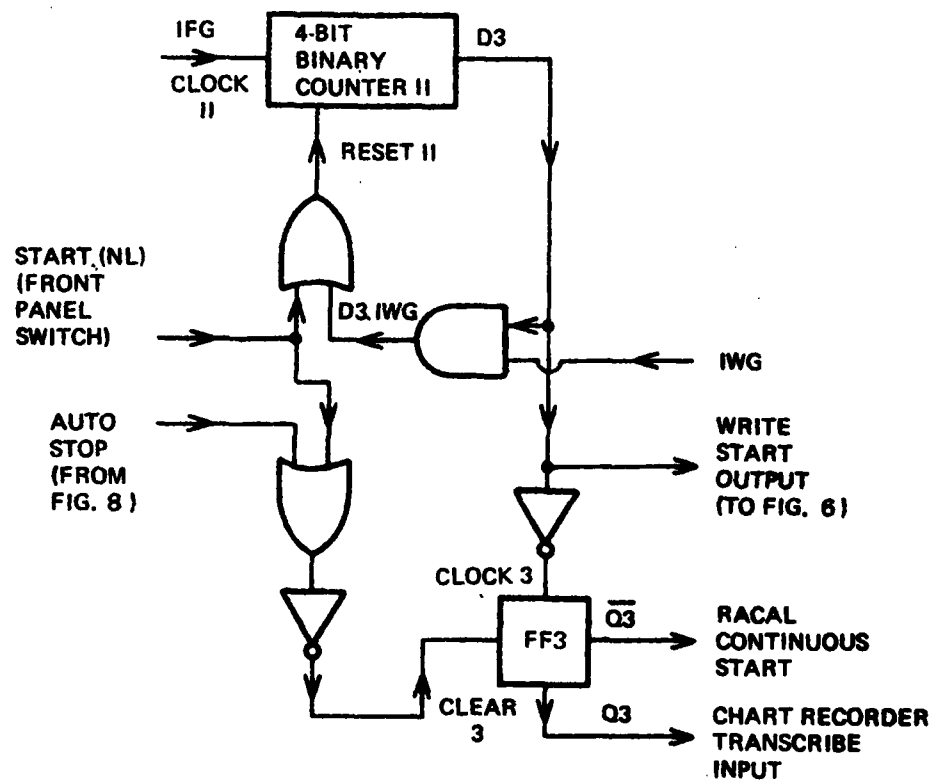FIG. 3(b) INPUT CONTROL CIRCUIT — PART 2

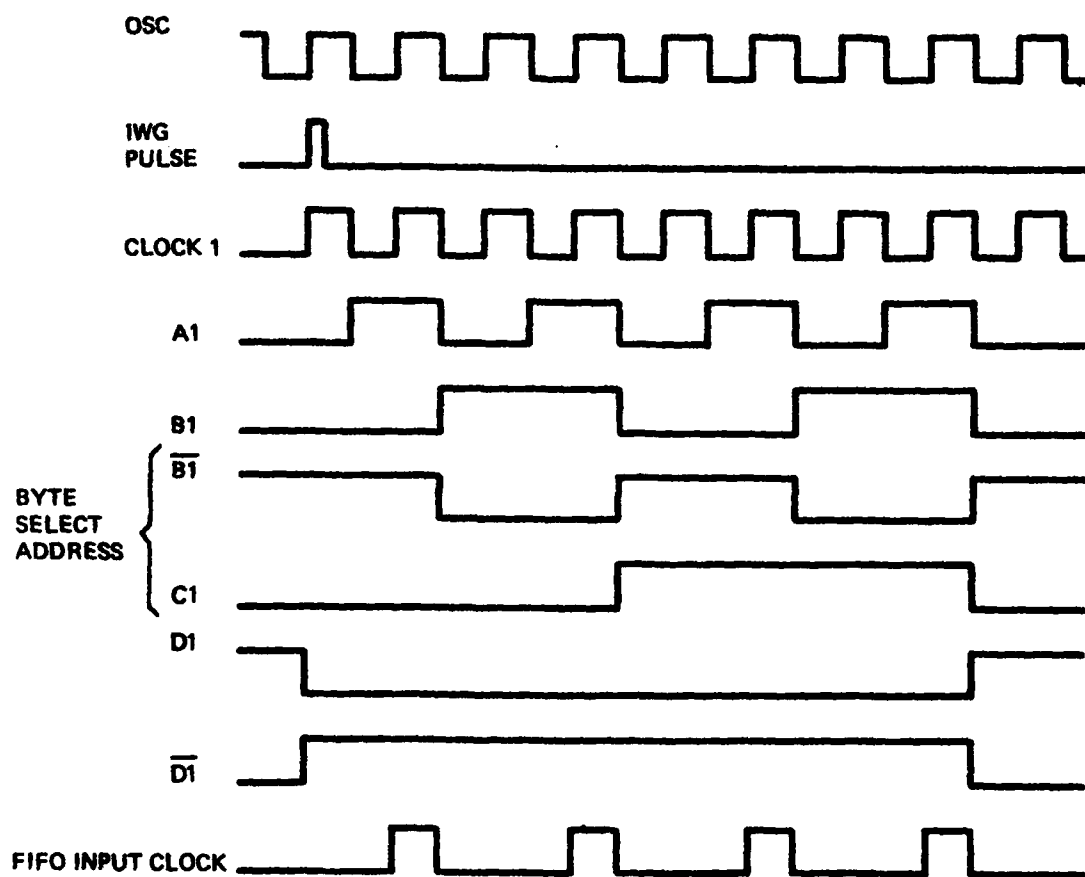FIG. 3(c) INPUT CONTROL CIRCUIT — PART 3

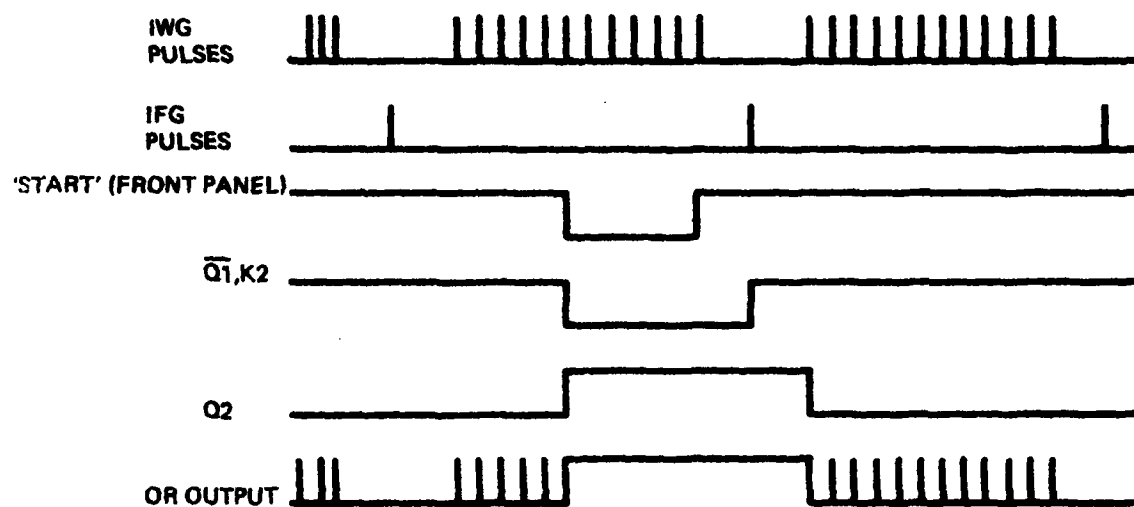FIG. 4(a) INPUT CONTROL CIRCUIT, PART 1 — TIMING DIAGRAM

FIG. 4(b) INPUT CONTROL CIRCUIT, PART 2 — TIMING DIAGRAM
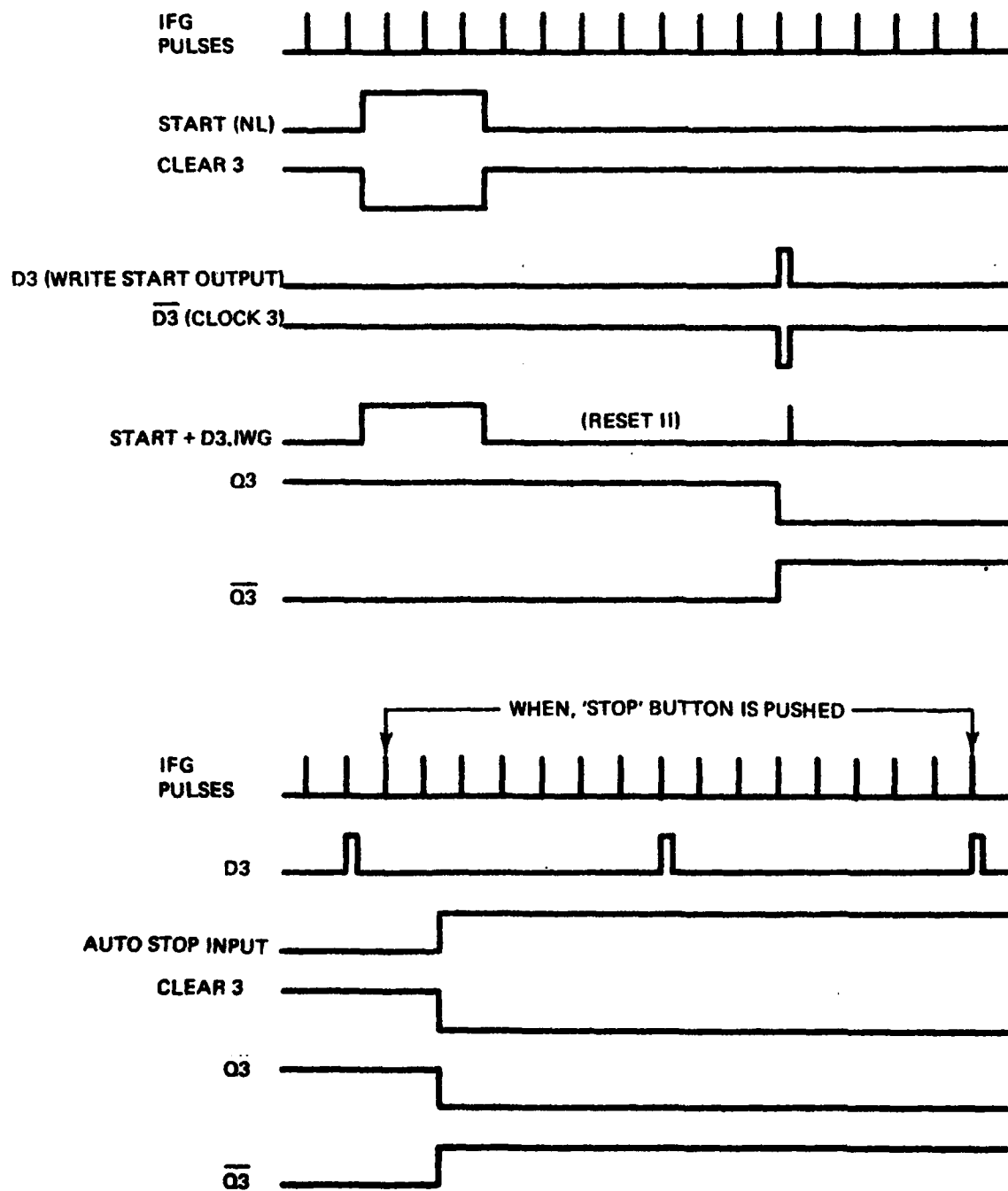
FIG. 4(c) INPUT CONTROL CIRCUIT, PART 3 — TIMING DIAGRAM

FROM DECODER

TRACK 1   TRACK 2

12-BIT WORD   12-BIT WORD

A   B   A   B   6-BIT BYTES

[A IS MOST SIG. BYTE
B IS LEAST SIG. BYTE]

FROM INPUT CONTROL CIRCUIT PART 1 { $\overline{B1}$, C1 }

BYTE SELECTOR

6—BIT OUTPUT BYTE (SEE TABLE BELOW)

TO FIFO INPUT

BYTE SELECT ADDRESS		OUTPUT BYTE	
B1	C1	TRACK	BYTE
1	0	1	A
0	0	1	B
1	1	2	A
0	1	2	B

FIG. 5   BYTE SELECTOR SEQUENCE

FROM DECODER

TRACK 1   TRACK 2

12-BIT   12-BIT
WORD   WORD

A   B   A   B   ← 6-BIT
                                               BYTES

                                             ⎡ A IS MOST SIG. BYTE ⎤
                                             ⎣ B IS LEAST SIG. BYTE ⎦

FROM $\overline{B1}$
INPUT
CONTROL   BYTE
CIRCUIT   SELECTOR
PART 1   C1

                                             6-BIT
                                             OUTPUT BYTE
                                             (SEE TABLE
                                             BELOW)

TO FIFO INPUT

BYTE SELECT ADDRESS		OUTPUT BYTE	
B1	C1	TRACK	BYTE
1	0	1	A
0	0	1	B
1	1	2	A
0	1	2	B

FIG. 5   BYTE SELECTOR SEQUENCE

FIG. 6   OUTPUT CONTROL CIRCUIT — PART 1

WRITE
START

QM1

Q4/J5

Q4/J5

Q5

OSC.Q5

OSC.Q5

Q6

QM2

QM3

FIG. 7   OUTPUT CONTROL CIRCUIT, PART 1 – TIMING DIAGRAM

GAP PULSE (FROM OUTPUT
CONTROL CIRCUIT
— PART 1)

+5V
'STOP'

$\overline{QM4}$

IRG

TO
RACAL

ANTI
BOUNCE

MONOSTABLE
4

150 ms

QM4

EOF

+5V
'START'

J6   K6

FF6   Q6

CLOCK
6

AUTO STOP
(TO INPUT
CONTROL CIRCUIT
— PART 3)
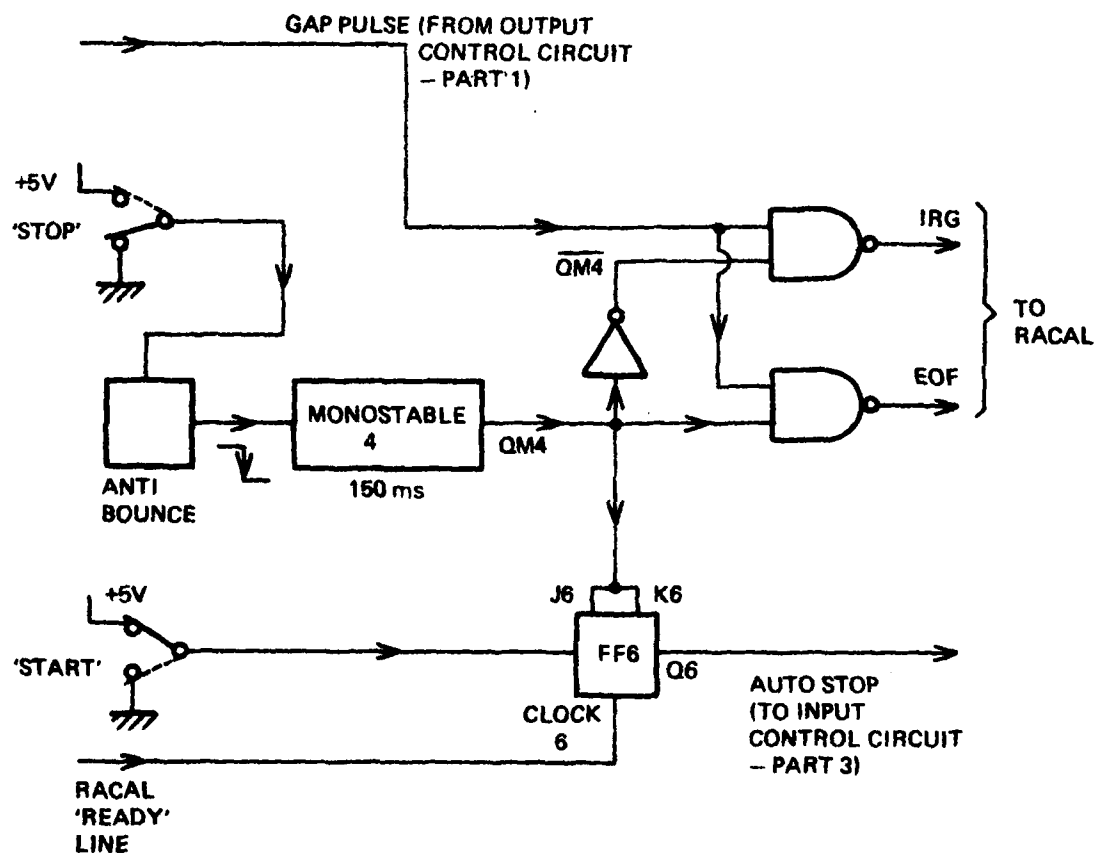
RACAL
'READY'
LINE

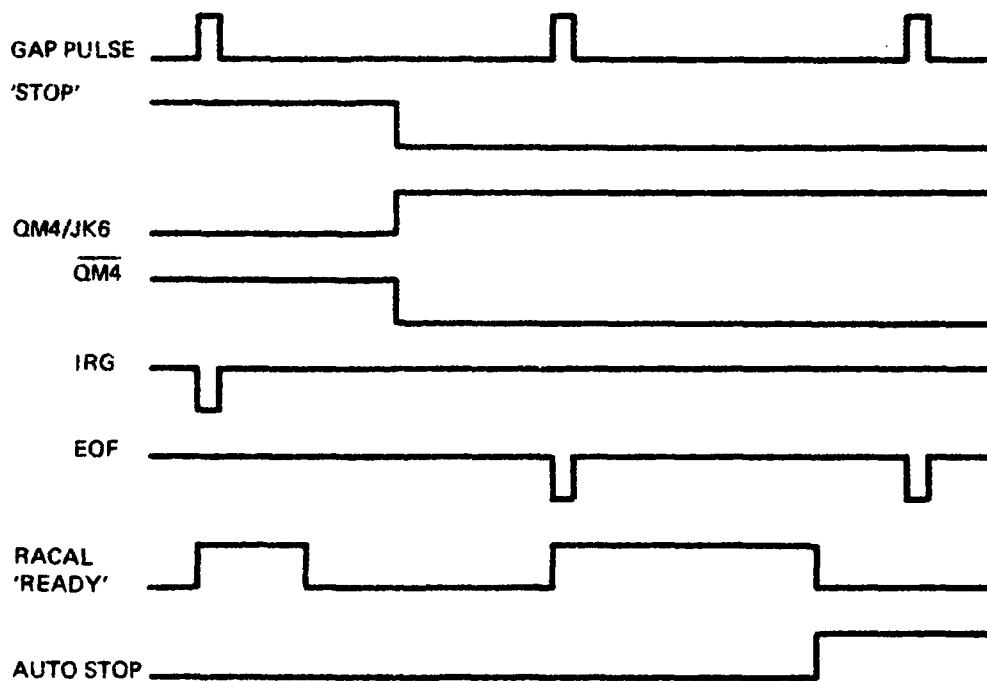FIG. 8   OUTPUT CONTROL CIRCUIT, PART 2

FIG. 9   OUTPUT CONTROL CIRCUIT, PART 2 — TIMING DIAGRAM

FIG. 10 TEST GENERATOR, PART 1

GATED
CLOCK
(FROM PART 1)

FROM
PART 1

NL

RESET

4-BIT
BINARY
COUNTER 8

CLOCK 8

B8   C8   D8

MONO 5
INHIBIT
(TO PART 1)

C8.D8

$\overline{C8.D8}$

MONOSTABLE
6

QM6

TEST
IWG
PULSE

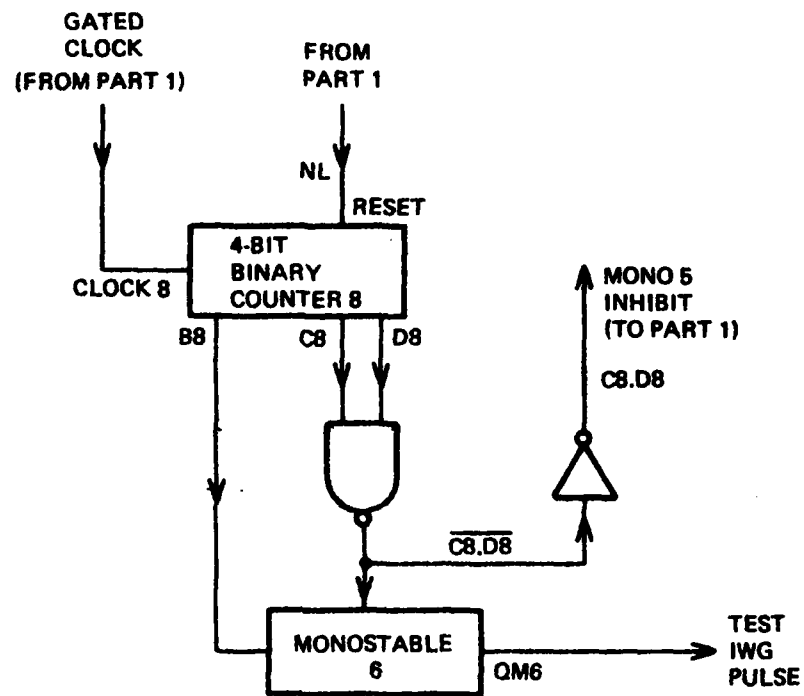**FIG. 11   TEST GENERATOR, PART 2**
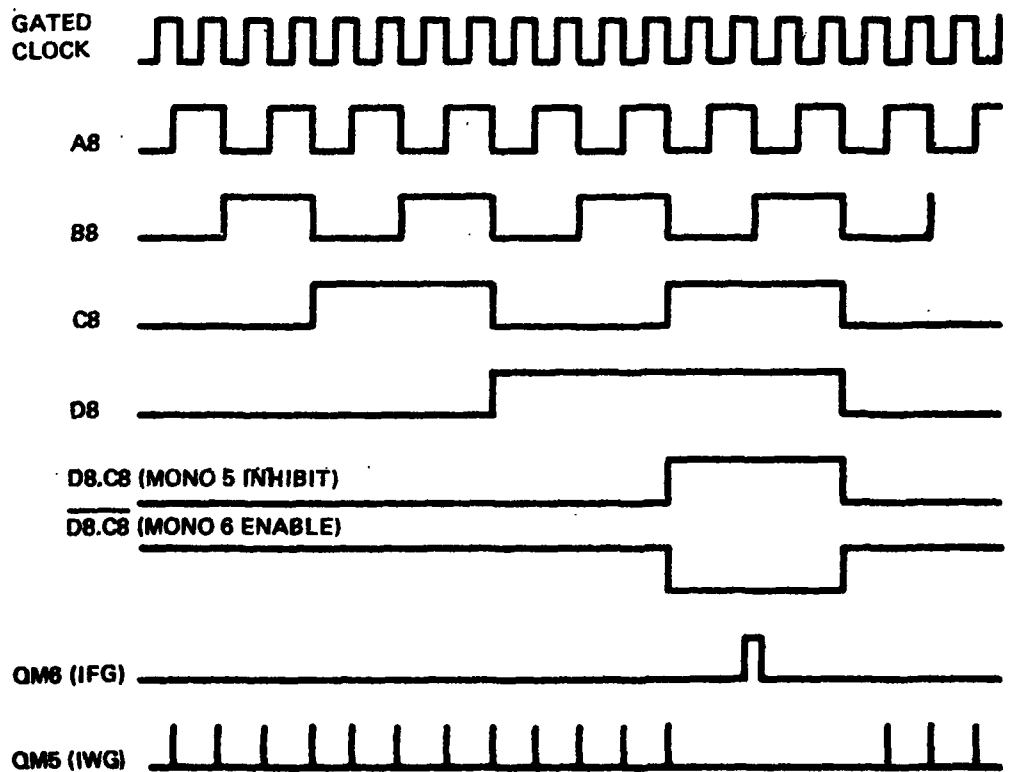
FIG. 12   TEST GENERATOR, PART 2 — TIMING DIAGRAM

TRANSFORMER
POWER SUPPLY
FIFO STACK
BYTE SELECTOR
OUTPUT CONTROL
INPUT CONTROL
TEST GENERATOR

DECODING

TOP VIEW

M8 SIZE PCB

M21 SIZE PCB

ON/OFF

START

NOT USED
TR1 DATA INPUT
TR1 TEST DATA OUTPUT
TR1 DECODED DATA OUTPUT
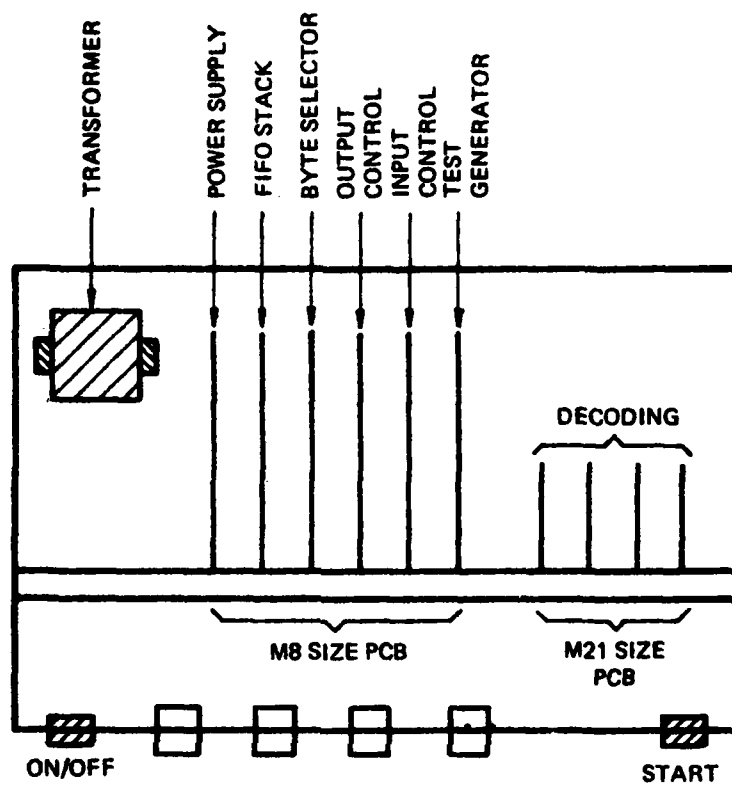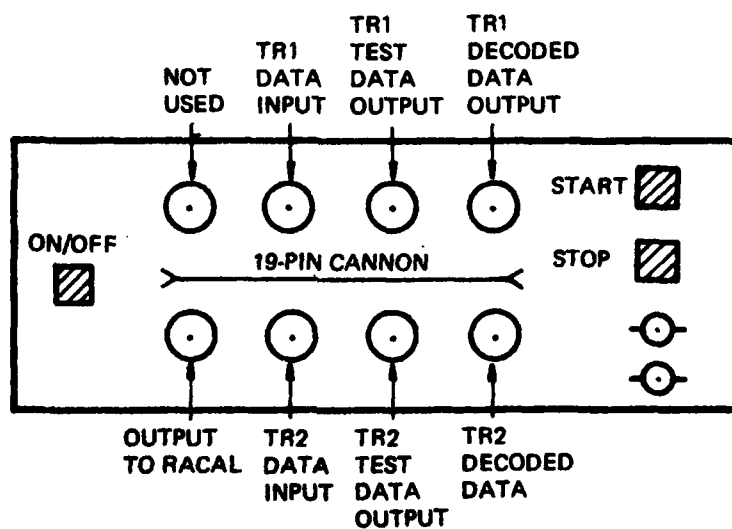
ON/OFF

START

STOP

FRONT VIEW

19-PIN CANNON

OUTPUT TO RACAL
TR2 DATA INPUT
TR2 TEST DATA OUTPUT
TR2 DECODED DATA

FIG. 13   MECHANICAL LAYOUT

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